ABSTRACT OF THE DISCLOSURE

There is provided a UTOPIA level interface in an ATM multiplexing/demultiplexing assembly, in which a multiplexer supporting UTOPIA level 2 and a processor supporting UTOPIA level 1 in the ATM multiplexing/demultiplexing assembly of the BIS are constructed of a single electrically programmable logic device (EPLD) to realize high-speed information exchange and simplify the configuration of the assembly. The ATM multiplexing/demultiplexing assembly includes the multiplexer for supporting the UTOPIA level 2 and executing an ATM layer function and the processor for performing the ATM layer function and supporting the UTOPIA level 1. The UTOPIA level interface comprises a UTOPIA interface controller for carrying out an ATM physical layer function to interface the layers of the multiplexer and the processor with each other and for performing level interface between the UTOPIA level 1 and UTOPIA level 2 to provide a 16-bit data path.